Deep Learning for Intelligent Wafer Defect Pattern Recognition System

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Abstract

Modern electronic manufacturing production lines embed several processes including among these, the electric wafer testing phase (EWS i.e. Electrical Wafer Sorting). The EWS validation phase includes the execution of several electrical tests directly on the integrated circuits over the wafer. The electrical assessment of EWS session can be reported in 2D binary map enabling the need to process these digital maps properly. Specifically, from this intelligent EWS analysis it is possible to early-identify defects in the production lines, electrical defects in the devices and finally,forecast proper wafer yield estimation. The detection and classification of the patterns in the EWS maps is a very challenging and time-consuming task. In the context of a joined research activity inside STMicroelectronics in collaboration with University of Catania, ad-hoc deep learning solution has been developed in order to perform supervised/unsupervised EWS maps pattern recognition and tracking.

1 Introduction

The current global chip shortage brought manufactories to find solutions to improve the production yield of microelectronic devices. The development of end-to-end machine learning pipelines daily scheduled in the production environment enable experts to spot anomalies or patterns in the development product process. Specifically, the critical phase related to electrical validation of the wafer (EWS i.e. Electrical Wafer Sorting), requires proper and experienced effort. More in detail, the analysis of the EWS image-map which embeds an imaging planar representation of the devices distribution over the wafer, needs a considerable effort. In this work, the authors refer to a EWS binary map i.e. a 2D binary image which reports good and bad device-dies as outcome of electrical testing. More in detail, the EWS binary map report a "0" value to show a good die i.e. die which has passed all the scheduled electrical tests, while the value "1" is assigned to a bad device-die which has failed some of the performed electrical tests.

The time-consuming analysis performed by experts (however impacted by the subjective experience of the operator) for analyzing aforementioned EWS maps show such typical limits of a manually performed process with outcomes that often include errors, omissions or incorrect assessments. In the context of a research collaboration between the STMicroelectronics R&D Power and Discretes division and the PerCeiVe Lab of the University of Catania, the authors developed a deep learning algorithms for automatic/intelligent EWS map management applied to a specific automotive products based on classical silicon materials as well as on Silicon Carbide (SiC). Currently, Silicon Carbide (SiC) finds wide application in the semiconductor industry thanks to its electrical characteristics, which distinguish it from silicon for potential applications in high power, high frequency and high temperature devices. Not surprisingly, this material finds its main application in the development of devices for the electric car. The current limit to its diffusion is given by the quality of the starting material or rather, of the substrates processed to arrive at the final device. Technological processes and wafer sizes related to SiC are therefore different from those based on classical silicon material. In this work we refer both to silicon and SiC wafers for automotive applications.

2 EWS Testing: Description

The work herein described has been tested on the following three datasets: WM811K, MixedWM38 and a dataset which contain internal STMicroelectronics EWS binary maps.

- WM811K was created by Taiwan Semiconductor Manufacturing Company [Wu et al., 2015]: it contains about 811,000 wafer maps and 9 patterns (Fig. 1). This dataset is unbalanced as it is based on RGB images of different resolution showing an overexpressed class with 176,000 samples of "none" classified pattern;
  MixedWM38 [Wang et al., 2020] contains 38,015 EWS wafer maps showing 38 different patterns as combination of 9 base-patterns quite similar to the ones included in the WM811K dataset. Unlike the aforementioned dataset, the MixedWM38 dataset includes class-balanced 52x52 RGB images representing the main EWS patterns such as

"Near-full", "Random", "Center", "Edge-Loc", "Scratch" and so on.

- The EWS maps dataset created by STMicroelectronics which contains silicon and SiC EWS images showing several classic and custom patterns identified in the internal production lines. The dataset includes 61x61 RGB images for a total of 6,732 samples. Some instances on Fig. 1.

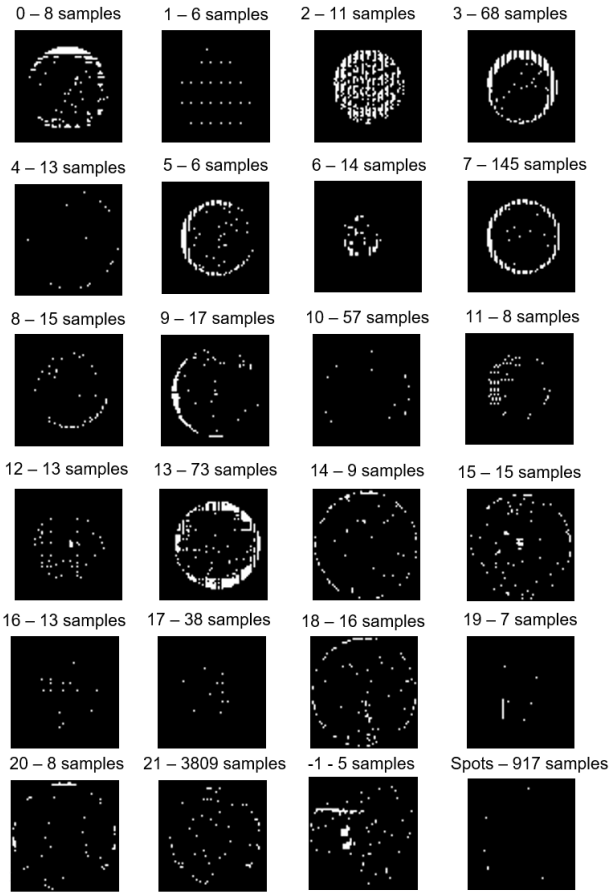

Figure 1. STMicroelectronics EWS maps dataset

We have trained and tested our depp algorithm development on the whole dataset which includes all the aforementioned dataset with a total of 70.266 images and 45 EWS pattern classes. The proposed deep learning algorithm embeds a supervised pipeline for labeled EWS map detection as well as unsupervised parallel pipeline for intelligent clustering of novel EWS patterns.

3 EWS map intelligent management: Supervised pipeline

The supervised EWS-map pattern recognition sub-system embeds ad-hoc designed deep convolutional network trained on the whole dataset (all the images have been converted to grayscale and resized to 61x61) using hold-out split (80 for training and 10/10 for testing and validation) [Kolesnikov et al., 2021]. In Fig. 2 we reported the overall scheme of the proposed supervised pipeline. The developed ad-hoc CNN has been compared with different backbones. We have also designed and tested a novel and customized viual-transformer based architecture [Kolesnikov et al., 2021]. The experimental results reported in Table 1 and 2 confirmed the effectiveness of the implemented deep pipeline.

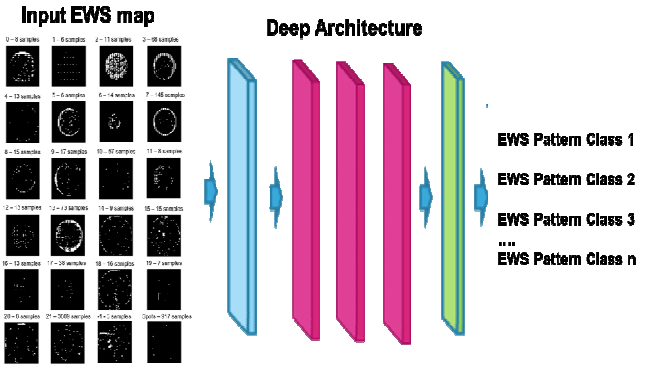

Figure 2. The proposed supervised EWS map classification deep pipeline

Model	Epoch	Training	Validation	Test
Deep CNN	**67**	**0.9766**	**0.9643**	**0.9683**

Table 1: Supervised EWS map classification -Deep CNN- experimental performance

As showed in Table 2, Visual transformer (ViT) and the designed Deep CNN showed very interesting performance in the EWS pattern classification (in terms of F1-score index). The results outperformed the pipelines proposed in scientific literature and applied in the same dataset we used in this work [Wu et al., 2015; Wang et al., 2020;]

	Deep CNN	ViT
Pattern	F1-Score	F1-score
Near-full	0.96	0.97
cluster_11	0.96	0.93
cluster_23	0.99	0.95
cluster_27	0.91	0.81
cluster_38	1.00	1.00
cluster_40	**0.80**	**0.43**
cluster_44	0.99	0.99
cluster_70	**0.59**	**0.27**

Table 2: EWS-map classification experimental benchmark

3.1 EWS map intelligent management: Unsupervised pipeline

Although the proposed supervised deep learning solution showed very interesting results, we decided to cover the scenario in which novel and not previously classified patterns were showed in the analyzed EWS maps. Classical approaches proposed in scientific literature implemented

Principal Component Analysis (PCA) and K-means based solutions. Anyway, both PCA and K-means methods confirmed low performance and reduced accuracy in that topic. In this context, the authors have proposed an innovative solution which uses custom and proprietary high-dimensional connected graph for performing intelligent unsupervised clustering of the input analyzed EWS map patterns. We tested the implemented unsupervised solution in a dataset of 12.696 EWS binary 61x61 RGB maps without apriori classification. The performed clustering shows very interesting performance as confirmed in the applications of the algorithm in the STMicroelectronics product lines. A preliminary evaluation of the more predominant EWS patterns translated into 3D surface plot is reported in Fig. 3. Some clustered EWS patterns related to SiC devices are reported in Fig. 4.

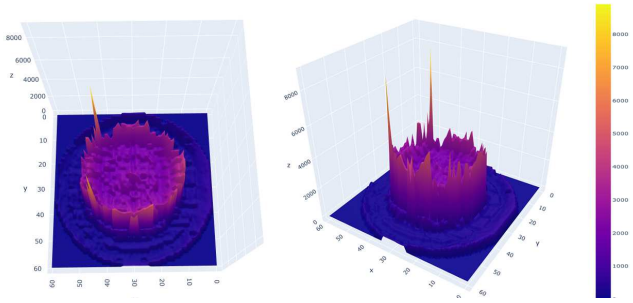

Figure 23. 3D rendering of SiC wafer maps

4 Conclusion

The usage of deep learning algorithms both supervised and unsupervised for EWS binary maps classification/clustering can be effective used to help manufacturing to improve the production yield. By means of an accurate control of the indicative EWS patterns of defects or anomalies in the production lines and of the correlations with the yield, it is possible to monitor the production processes for both silicon and SiC devices. As part of a research framework agreement between STMicroelectronics and the University of Catania, further developments of innovative solutions are underway for the realization of the so-called smart intelligent factory mainly related to automotive deliverables.

References

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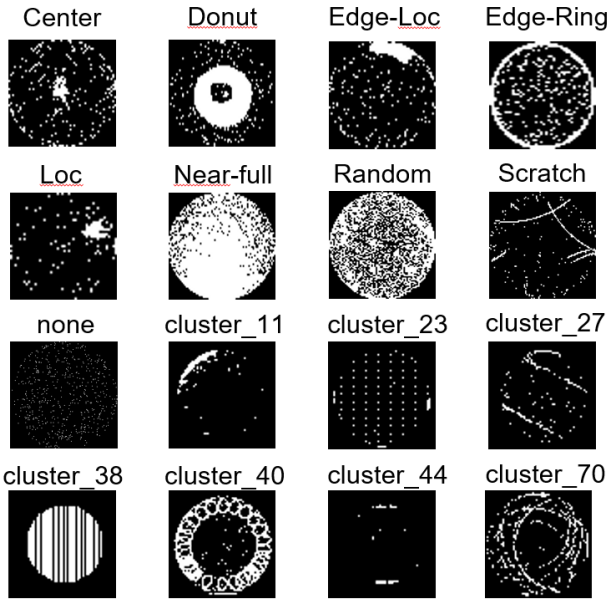

Figure 4. Clustering results over internal STMicroelectronics SiC Dataset